TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 19378.0026

US APPLICATION NO (If known, see 37 CFR 1 5): 10/088691

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/SE00/01847	22 September 2000	22 September 1999

TITLE OF INVENTION: A COMPUTER DEVICE WITH A SAFETY FUNCTION

APPLICANT(S) FOR DO/EO/US: Marieanne Almesåker and Bengt Nyström

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. [x] This is a **FIRST** submission of items concerning a filing under 35 U S.C. 371
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C § 371
3. [x] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U S.C 371(b) and PCT Articles 22 and 39(1).
4. [x] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. [x] A copy of the International Application as **published** (35 U.S.C 371(c)(2))**WO 01/22220**
   a. [x] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2))

7. [x] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a [x] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U S.C. 371(c)(3).

9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4))

10. ☐ A translation of the Annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S C. 371(c)(5)).

Items 11. to 16. Below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3 28 and 3.31 is included

13. [x] A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter

16. [x] Other items or information.

PCT/ISA/210
PCT/IB/332
PCT/IPEA/409

U.S. APPLICATION NO (If known, see 37 CFR 1 5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
10/088691	PCT/SE00/01847	19378.0026

JC13 Rec'd PCT/PTO 21 MAR 2002

X The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO..... **$890.00**		
International preliminary examination fee paid to USPTO (37 CFR 1 482) **$710.00**		
No international preliminary examination fee paid to USPTO (37 CFR 1 482) but international search fee paid to USPTO (37 CFR 1 445(a)(2))..... **$740.00**		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$1,040.00**		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	**$1,040.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 [x] 30 months from the earliest claimed priority date (37 CFR 1.492(c))	**$ 130.00**	

Claims	Number Filed	Number Extra	Rate		
Total Claims	14 - 20 =	0	X **$18.00**	**$**	
Independent Claims	3 - 3 =	0	X **$84.00**	**$**	
Multiple dependent claim(s)(if applicable)			+ **$280.00**	**$**	
TOTAL OF ABOVE CALCULATIONS =				**$1,170.00**	
Reduction by 1/2 for filing by small entity, if applicable.				**$**	
SUBTOTAL =				**$1,170.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1 492(e)).				**$**	
TOTAL NATIONAL FEE =				**$1,170.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				**$**	
TOTAL FEES ENCLOSED =				**$1,170.00**	
				Amount to be: Refunded	**$**
				Charged	**$1,170.00**

a. ☐ A check in the amount of $___ to cover the above fees is enclosed.

b. [x] Please charge my Deposit Account No. **19-5127; 19378.0026** in the amount of **$1,170.00** to cover the above fees
A duplicate copy of this sheet is enclosed.

c. [x] The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **19-5127**. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status

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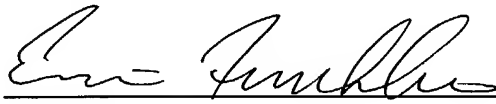

SIGNATURE
Eric J. Franklin
NAME
37,134
REGISTRATION NUMBER

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
Marieanne Almesåker et al.	:	Attorney Docket: 19378.0026
Serial No.: To be assigned	:	Art Unit: To be assigned
Filed: Herewith	:	Examiner: To be assigned

For: A COMPUTER DEVICE WITH A SAFETY FUNCTION

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination, please amend the above-identified application as follows:

In the Claims:

Please amend the claims as follows:

Clean copy of amended claims:

4. A computer device according to claim 1, where in said supervisory unit (14) is arranged to generate a signal in dependence of a timer (18) in such a manner that said restart signal is generated if no trigger-signal signal that sets the timer (18) to zero is received within a predetermined time interval.

5. A computer device according to claim 1, comprising a memory safety circuit (20) that is arranged to stop the reading from the ordinary memory unit (12) and to connect for reading from said further memory unit (16) when both said restart signal and a signal indicating applied supply voltage is the case.

6. A computer device according to claim 1, wherein said further memory unit (16) is arranged such that it comprises basic system instructions with a high degree of reliability.

8. A computer device according to claim 1, wherein at least said further memory unit (16) is a non-volatile memory.

9. A computer device according to claim 1, wherein said processor means (10) comprises a working memory (22) that is arranged such that at a restart of the computer device this working memory (22) is reset before reading from said further memory unit (16) is started.

10. A computer device according to claim 1, arranged such that if said restart signal has been generated a predetermined number of times, then, in case an error occurs again, said stop signal is generated.

11. A computer device according to claim 1, comprising a switching member (24) for manually generating said restart signal.

14. Use of a computer device according to claim 1 for controlling a system that is included in an aircraft.

Amended claims:

4. (Amended) A computer device according to [any of the preceding claims] claim 1, where in said supervisory unit (14) is arranged to generate a signal in dependence of a timer (18) in such a manner that said restart signal is generated if no trigger-signal signal that sets the timer (18) to zero is received within a predetermined time interval.

5. (Amended) A computer device according to [any of the preceding claims] claim 1, comprising a memory safety circuit (20) that is arranged to stop the reading from the ordinary memory unit (12) and to connect for reading from said further memory unit (16) when both said restart signal and a signal indicating applied supply voltage is the case.

6. (Amended) A computer device according to [any of the preceding claims] claim 1, wherein said further memory unit (16) is arranged such that it comprises basic system instructions with a high degree of reliability.

8. (Amended) A computer device according to [any of the preceding claims] claim 1, wherein at least said further memory unit (16) is a non-volatile memory.

9. (Amended) A computer device according to [any of the preceding claims] claim 1,

wherein said processor means (10) comprises a working memory (22) that is arranged such that at a restart of the computer device this working memory (22) is reset before reading from said further memory unit (16) is started.

10. (Amended) A computer device according to [any of the preceding claims] claim 1, arranged such that if said restart signal has been generated a predetermined number of times, then, in case an error occurs again, said stop signal is generated.

11. (Amended) A computer device according to [any of the preceding claims] claim 1, comprising a switching member (24) for manually generating said restart signal.

14. (Amended) Use of a computer device according to [any of the claims 1-12] claim 1 for controlling a system that is included in an aircraft.

Remarks

Applicants have amended the claims to eliminate multiple dependencies and thereby reduce the filing fee.

Respectfully submitted,

Date: March 19, 2002

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1/pRTS

A COMPUTER DEVICE WITH A SAFETY FUNCTION

BACKGROUND OF THE INVENTION AND PRIOR ART

The present invention concerns a computer device with a safety function for avoiding non-necessary disconnection of the computer device, comprising processor means, an ordinary memory unit connected to said processor means and arranged to comprise at least one program that is executed by the processor means, a supervisory unit that supervises the function of the computer device and that is arranged to, in case an error occurs, send a restart signal or a stop signal to the processor means.

Such computer devices are already known. The supervisory unit may for instance constitute a so-called "watchdog timer". US-A-4 763 296 describes the function of such a watchdog timer. Such a device thus has a timer that continuously is in operation when the computer device is used. If the timer reaches a predetermined value, i.e. if a predetermined time has elapsed, the watchdog timer generates a restart signal that causes a restart (reset) of the computer device. During normal use, the timer is set to zero at regular intervals by the normal program execution by the processor. In case an error occurs, for example if the computer executes an infinite subroutine, the timer will not be set to zero and the watchdog timer thus causes a restart of the system.

Also other kinds of computer devices with safety functions are already known. EP-A-481 508 thus describes a device that comprises a backup memory. When the current supply to the computer device is shut off, the status of the central processor and the content in a main memory are transferred to said backup memory. When then the computer device is started once again by

again connecting the current supply, that which is stored in the backup memory will be restored.

EP-A-265 366 describes a computer device that comprises a primary memory and a backup memory. Switching from the primary memory to the backup memory is done by means of a "Backup Control System Transfer Mechanism". This mechanism is relatively complicated. At the generation of a power-on-reset signal, said mechanism secures that restart is done from the primary memory (see column 6, lines 21-28).

There exists a need to improve the safety function of a computer device. There is thus a need of in a safe manner restarting the computer device when an error has been detected. Such an error that may cause errors in the operation of the computer is for example memory errors that may occur in the memory where programs that are executed in the computer device are stored. An error may also be caused by the software that is stored in the memory of the computer device. Such errors may for example occur when new software is used that has not been completely tested. Furthermore, there exists a need to secure the function of the computer device by relatively simple means. A further problem is to secure at least certain basic functions of the computer device when different errors occur.

SUMMARY OF THE INVENTION

The purpose of the present invention is to achieve a computer device with a reliable safety function that, furthermore, is achieved by relatively simple means.

This purpose is achieved by the initially defined computer device that is characterised by a further memory unit that is arranged to comprise at least some basic system instructions, wherein the computer device is arranged such that the processor means, at a restart generated by said restart signal from the supervisory unit, is connected to the further memory unit and reads and executes

instructions that are stored in the same, while the ordinary memory unit is disconnected from the processor means.

By the fact that the processor means is connected to the further memory unit when a restart signal has been generated by the supervisory unit, it is avoided that possible errors that are present in the instructions that are stored in the ordinary memory unit are transferred to the processor means. A safer function of the computer device after that a restart signal has been generated in response to a detected error is thereby achieved. In this context it should be noted that when in the claims and in the description it is mentioned that a memory unit is connected to or is disconnected from the processor means, it is thereby not necessarily meant that the disconnection is done by physically breaking the connection between the processor means and the memory unit in question. The concepts connect to and disconnect thus comprise two possibilities: physical switching by breaking the connection, and the connection to and the disconnection from at a program level.

It should be noted that by the concept "system instructions" is in this application preferably, but not necessarily, meant programs that control a system or a part of a system that is controlled by the computer device, i.e. the concept "system instructions" concerns application instructions.

According to an embodiment of the invention, the ordinary memory unit and the further memory unit constitute two different, physically separate, memories. By this feature an increased security is achieved since the ordinary memory unit is arranged as a separate memory that is completely disconnected from the processor means at a restart.

According to an alternative embodiment of the invention, the ordinary memory unit and the further memory unit constitute two parts of physically the same memory, but with different memory addresses. Through this construction fewer memory components

are needed since the further memory unit is stored as a special part of the memory where also the ordinary memory unit is included.

According to a further embodiment of the invention, said supervisory unit is arranged to generate a signal in dependence of a timer in such a manner that said restart signal is generated if no trigger signal that sets the timer to zero is received within a predetermined time interval. The supervisory unit may in this case thus constitute a so-called watchdog timer (WDT). Such a WDT often forms part of computer devices. Such a well functioning and already existing WDT may thus be used as a supervisory unit in the device according to the present invention. It should however be noted that also other kinds of supervisory units than a WDT may be used in the computer device according to the invention.

According to still another embodiment of the invention, the computer device comprises a memory safety circuit that is arranged to stop the reading from the ordinary memory unit and to connect for reading from said further memory unit when both said restart signal and a signal indicating applied supply voltage is the case. Such a memory safety circuit is a relatively simple and well functioning circuit that controls that switching from the ordinary to the further memory unit takes place. Furthermore, this memory safety circuit secures that such a switching only occurs if supply voltage to the computer device is present.

According to a further embodiment of the invention, said further memory unit is arranged such that it comprises basic system instructions with a high degree of reliability. The further memory unit may hereby be arranged to comprise system instructions that have already been thoroughly tested and that therefore have a high functional reliability. The further memory unit may hereby also be provided with the basic system instructions for the computer device while non-necessary system instructions have been excluded from said further memory unit.

According to still another embodiment of the invention, said further memory unit is arranged such that it comprises system instructions with a degree of reliability that is higher than the degree of reliability that is the case in the ordinary memory unit. The ordinary memory unit may thus comprises system instructions that have not been so thoroughly tested in the computer device. The further memory unit may thereby comprise the basic system instructions that have already been shown to have a high reliability. Within the frame of the invention is of course also the possibility that the ordinary memory unit and the further memory unit comprise system instructions with the same degree of reliability.

According to a further embodiment of the invention, at least said further memory unit is a non-volatile memory. This fact contributes to an increased functional reliability of the computer device.

According to still another embodiment of the invention, said processor means comprises a working memory that is arranged such that at a restart of the computer device this working memory is reset before reading from said further memory unit is started. By this feature is secured that instructions that may comprise errors and that originate from the ordinary memory unit do not maintain in the working memory before reading from the further memory unit is started.

According to a further embodiment of the invention, said further memory unit is arranged to be write protected at least when the computer device is in operation. This fact contributes to further safety since the content in this further memory unit is protected and may not be modified when the computer device is in operation.

According to still another embodiment of the invention, the computer device is arranged such that if said restart signal has been generated a predetermined number of times, then, in case an error occurs again, said stop signal is generated. This means that the supervisory unit generates a predetermined number of restart signals. If it happens that an error is the case even after that a

predetermined number of restart attempts have been made, the computer device is stopped.

According to still another embodiment of the invention, the computer device comprises a switching member for manually generating said restart signal. This means that in addition to automatic generation of a restart signal by the supervisory unit, also a manual restart signal may be generated by an operator. An operator may thus order that a restart from the further memory unit is to take place.

A further embodiment of the invention is clear from claim 13. This embodiment may also be combined with the features of one or more of the claims 2-12.

The purpose of the invention is also achieved by a method according to claim 14. This method has advantages corresponding to those described in connection with the device. The method according to claim 14 may also be combined with features corresponding to those defined in one or more of the claims 2-12.

A preferred use of the computer device is to use it to control a system that is included in different vehicles, for example in aircrafts. An aircraft has many different functions that are controlled by a computer device. It is important that these functions function and that unnecessary disconnection of the computer device or of its operation concerning some application is avoided. This aim is achieved by a use according to claim 15.

SHORT DESCRIPTION OF THE DRAWING

The present invention will now be explained by means of a described embodiment, which constitutes an example of the invention, and with reference to the annexed drawing.

Fig 1 shows schematically a block diagram of an embodiment of the invention.

DETAILED DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

Fig 1 shows a block diagram of an embodiment of the invention. The computer device comprises a processor means 10. With this processor means 10 is meant not only the central processor unit (CPU) of the computer device but also other central parts of the computer device such as for example the working memory 22. The computer device also comprises an ordinary memory unit 12. This ordinary memory unit 12 may for example constitute some kind of PROM, for example UVPROM, EEPROM or the like. When the computer device first is started, the processor means 10 is connected to the ordinary memory unit 12. This ordinary memory unit 12 is thus arranged to comprise the instructions that control the operation of the computer device. The computer device also comprises a supervisory unit 14. The supervisory unit 14 supervises the function of the computer device and is arranged to generate a restart signal or a stop signal to the processor means 10 if the supervisory unit 14 detects an error. The supervisory unit 14 may for example constitute a so-called watchdog timer (WDT). Such a WDT 14 generates a signal that depends on a timer 18. A restart signal is thereby generated if the WDT 14 within a predetermined time interval does not receive a trigger-signal that sets the timer 18 to zero. In order to have a high reliability, the WDT 14 comprises suitably its own timer 18. It is however possible that the timer function of the WDT 14 is controlled by the same clock that is included in the processor means 10.

The computer device also comprises a further memory unit 16. This further memory unit 16 is arranged to comprise at least some basic system instructions. The further memory unit 16 may constitute a memory that is physically separated from the ordinary memory unit 12. It is also possible that the ordinary memory unit 12 and the further memory unit 16 constitute two parts of physically the same memory. In order to further increase the reliability in case a memory error should occur, the ordinary memory unit 12 and the further

memory unit 16 may constitute physically separate memories of different kinds, for example from different manufacturers. The further memory unit suitably constitutes some kind of PROM, for example UVPROM or EEPROM.

The computer device also comprises a memory safety circuit 20. This memory safety circuit 20 may form a part of the processor means 10. In the shown embodiment, the memory safety circuit 20 however constitutes a separate circuit. The memory safety circuit 20 comprises an AND-gate 21. The memory safety circuit 20 controls which of the ordinary memory unit 12 and the further memory unit 16 that is to be connected to the processor means 10. This control may either be formed by opening or closing the electric connection between the respective memory unit 12, 16 and the processor means 10 or also be formed by a control on a program level of these connections. It is also possible that the control is done by a combination of software instructions and physically opening or closing. One input of the AND-gate is connected to a line 23 that indicates that a supply voltage is present. The other input of the AND-gate 21 is connected to a line 25 that is connected to the WDT 14. Via this line 25, a restart signal generated by the WDT 14 is lead to the AND-gate 21 and thereby to the memory safety circuit 20.

The computer device also comprises a switching member 24 for manually generating a restart signal. This switching member 24 may suitably be connected to the input of the AND-gate that is also connected to the WDT 14.

The WDT 14 thus supervises the function of the computer device. When the computer device functions normally, the WDT 14 receives at regular intervals a trigger-signal from the processor means 10. This trigger-signal sets the timer 18 to zero. The WDT 14 does thereby not generate any restart signal to the line 25. If, however, an error occurs such that the WDT 14 does not receive any trigger-signal from the processor means 10 within a predetermined time interval, the WDT 14 generates a restart signal. This restart signal

is thus lead to one of the inputs of the AND-gate 21. When the AND-gate 21 receives such a restart signal, and if at the same time the other input of the AND-gate 21 detects that a supply voltage is the case, the memory safety circuit 20 controls that the ordinary memory unit 12 is disconnected from the processor means 10 and that the further memory unit 16 is connected to the processor means 10. Also the processor means 10 receives a signal, suitably from the WDT 14, that a restart is to be performed. The working memory 22 of the processor means 10 is thereby reset, whereafter reading from the further memory unit 16 takes place. The reading is thereby done to predetermined addresses of the working memory 22. The processor means 10 thus reads and executes the instructions that are stored in the further memory unit 16.

It is conceivable that a restart attempt fails and that the WDT 14 thus generates a new restart signal. If again an error is detected, further restart signals may be generated by the WDT 14. The computer device is thereby suitably arranged such that when a predetermined number of restart attempts have been made, the restart attempts are stopped. A warning function may thereby be generated by the computer device and the latest information concerning the status of the processor means 10 and the memory units 12, 16 may be registered for later analysis. The computer device is suitably arranged such that the restart attempts are stopped after for example one to four restart attempts, preferably after two restart attempts. The computer device may thereby be arranged such that the restart attempts are stopped if said predetermined number of restart attempts have been performed within a predetermined time interval.

In order to increase the safety, the further memory unit 16 is suitably arranged such that it is write protected when the computer device is in operation. Furthermore, suitably the ordinary memory unit 12 as well as the further memory unit 16 constitute non-volatile memories.

The further memory unit 16 is suitably arranged such that it comprises basic system instructions with a high degree of reliability. The further memory unit 16 may thereby comprise primary and well-tested system functions. Suitably, the further memory unit 16 is arranged such that it thereby comprises system instructions with a higher degree of reliability than the system instructions that are present in the ordinary memory unit 12. By the expression "degree of reliability" may hereby for example be meant the software safety levels that are defined according to RTCA-standard document NO.RTCA/DO-178B.

The computer device according to the invention may preferably be arranged to secure the normal function of the computer device under the execution of an application program even when an error occurs that otherwise would lead to a disconnection and a shut-off of the computer device, or at least to the interruption of the execution of the application program in question. The ordinary memory unit 12 thus comprises an application program that is executed by the processor means 10. In case an error occurs in the execution of at least said application program, the processor means 10 is connected to the further memory unit 16 that is arranged to comprise at least some basic, already used and safe application instructions. The computer device is thus arranged such that the execution of the application that is controlled by the application program may continue on the basis of the application instructions that are retrieved from the further memory unit.

According to a method according to the invention, if an error occurs, a connection to the further memory unit 16 that comprises at least some basic application instructions takes place. The execution of the application that is controlled by an application program may thereby continue on the basis of the application instructions that are retrieved from the further memory unit and that are read in a normal and traditional manner into the processor means 10 with a normal reset of the working memory 22.

The computer device according to the invention may also advantageously be used to control a system that is included in an aircraft.

The present invention is not limited to the shown embodiment but may be varied and modified within the scope of the following claims.

Claims

1. A computer device with a safety function for avoiding non necessary disconnection of the computer device, comprising

processor means (10),

an ordinary memory unit (12) connected to said processor means (10) and arranged to comprise at least one program that is executed by the processor means (10),

a supervisory unit (14) that supervises the function of the computer device and that is arranged to, in case an error occurs, send a restart signal or a stop signal to the processor means (10),

characterised by

a further memory unit (16) that is arranged to comprise at least some basic system instructions, wherein the computer device is arranged such that the processor means (10) always at a restart generated by said restart signal from the supervisory unit (14) is connected to the further memory unit (16) and reads and executes instructions that are stored in the same, while the ordinary memory unit (12) is disconnected from the processor means (10), and wherein said further memory unit (16) is arranged to be write protected at least when the computer device is in operation.

2. A computer device according to claim 1, wherein the ordinary memory unit (12) and the further memory unit (16) constitute two different, physically separate, memories.

3. A computer device according to claim 1, wherein the ordinary memory unit (12) and the further memory unit (16) constitute two parts of physically the same memory, but with different memory addresses.

4. A computer device according to any of the preceding claims, wherein said supervisory unit (14) is arranged to generate a signal in dependence of a timer (18) in such a manner that said restart signal is generated if no trigger-signal signal that sets the timer (18) to zero is received within a predetermined time interval.

5. A computer device according to any of the preceding claims, comprising a memory safety circuit (20) that is arranged to stop the reading from the ordinary memory unit (12) and to connect for reading from said further memory unit (16) when both said restart signal and a signal indicating applied supply voltage is the case.

6. A computer device according to any of the preceding claims, wherein said further memory unit (16) is arranged such that it comprises basic system instructions with a high degree of reliability.

7. A computer device according to claim 6, wherein said further memory unit (16) is arranged such that it comprises system instructions with a degree of reliability that is higher than the degree of reliability that is the case in the ordinary memory unit (12).

8. A computer device according to any of the preceding claims, wherein at least said further memory unit (16) is a non-volatile memory.

9. A computer device according to any of the preceding claims, wherein said processor means (10) comprises a working memory (22) that is arranged such that at a restart of the computer device this working memory (22) is reset before reading from said further memory unit (16) is started.

10. A computer device according to any of the preceding claims, arranged such that if said restart signal has been generated a predetermined number of times, then, in case an error occurs again, said stop signal is generated.

11. A computer device according to any of the preceding claims, comprising a switching member (24) for manually generating said restart signal.

12. A computer device arranged to secure the normal function of the computer device under the execution of at least one application program also when an error occurs that normally leads to

disconnection and shut-off of the computer device or at least to disconnection concerning said application program, which computer device comprises
processor means (10), an ordinary memory unit (12) connected to said processor means (10) and arranged to comprise at least an application program that is executed by the processor means (10),
a supervisory unit (14) that supervises the function of the computer device and that is arranged to, in case an error occurs in the execution of at least said application program, send a restart signal or a stop signal to the processor means (10),
characterised by
a further memory unit (16) that is arranged to comprise at least some basic application instructions, wherein the computer device is arranged such that always when a restart takes place in response to a restart signal generated by the supervisory unit (14), the processor means (10) is connected to the further memory unit (16) and reads and executes instructions that are stored in the same, while the ordinary memory unit (12) is disconnected from the processor means (10), wherein the computer device is arranged such that the execution of the application that is controlled by said application program may continue on the basis of the application instructions that are retrieved from the further memory unit, wherein the execution of the application in question may continue without the necessity for the computer device to be disconnected, and wherein said further memory unit (16) is arranged to be write protected at least when the computer device is in operation.

13. A method for securing the normal function of a computer device under the execution of at least one application program also when an error occurs that normally leads to disconnection and shut-off of the computer device or at least to disconnection concerning said application program, which computer device comprises
processor means (10),
an ordinary memory unit (12) connected to said processor means (10) and arranged to comprise at least one application program that is executed by the processor means (10),

a supervisory unit (14) that supervises the function of the computer device and that is arranged to, in case an error occurs in the execution of at least said application program, send a restart signal or a stop signal to the processor means (10),

a further memory unit (16) that is arranged to comprise at least some basic application instructions, wherein said further memory unit (16) is arranged to be write protected at least when the computer device is in operation,

which method comprises that always when a restart takes place in response to a restart signal generated by the supervisory unit (14), the processor means (10) is connected to the further memory unit (16) and reads and executes instructions that are stored in the same, while the ordinary memory unit (12) is disconnected from the processor means (10), wherein the execution of the application that is controlled by said application program may continue on the basis of the application instructions that are retrieved from the further memory unit such that the execution of the application in question may continue without the necessity for the computer device to be disconnected.

14. Use of a computer device according to any of the claims 1-12 for controlling a system that is included in an aircraft.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 March 2001 (29.03.2001)

PCT

(10) International Publication Number
WO 01/22220 A1

(51) International Patent Classification[7]: G06F 9/445, 11/00, 11/30

(21) International Application Number: PCT/SE00/01847

(22) International Filing Date:
22 September 2000 (22.09.2000)

(25) Filing Language: Swedish

(26) Publication Language: English

(30) Priority Data:
9903422-5 22 September 1999 (22.09.1999) SE

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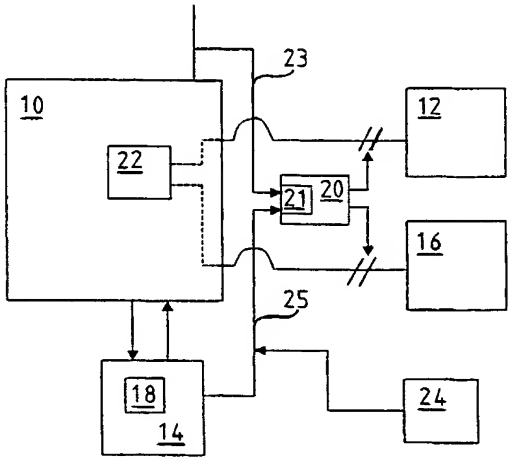
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, CZ (utility model), DE, DE (utility model), DK, DK (utility model), DM, DZ, EE, EE (utility model), ES, FI, FI (utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (utility model), SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A COMPUTER DEVICE WITH A SAFETY FUNCTION



(57) Abstract: The invention concerns a computer device with a safety function in order to avoid non-necessary disconnection of the computer device. The computer device comprises processor means (10), an ordinary member unit (12), a supervisory unit (14) and a further member unit (16). The computer device is arranged such that the processor means (10) at a restart generated by a restart signal, is connected to the further memory unit (16) and reads and executes the instructions that are stored in the same, while the ordinary memory unit (12) is disconnected from the processor means (10).

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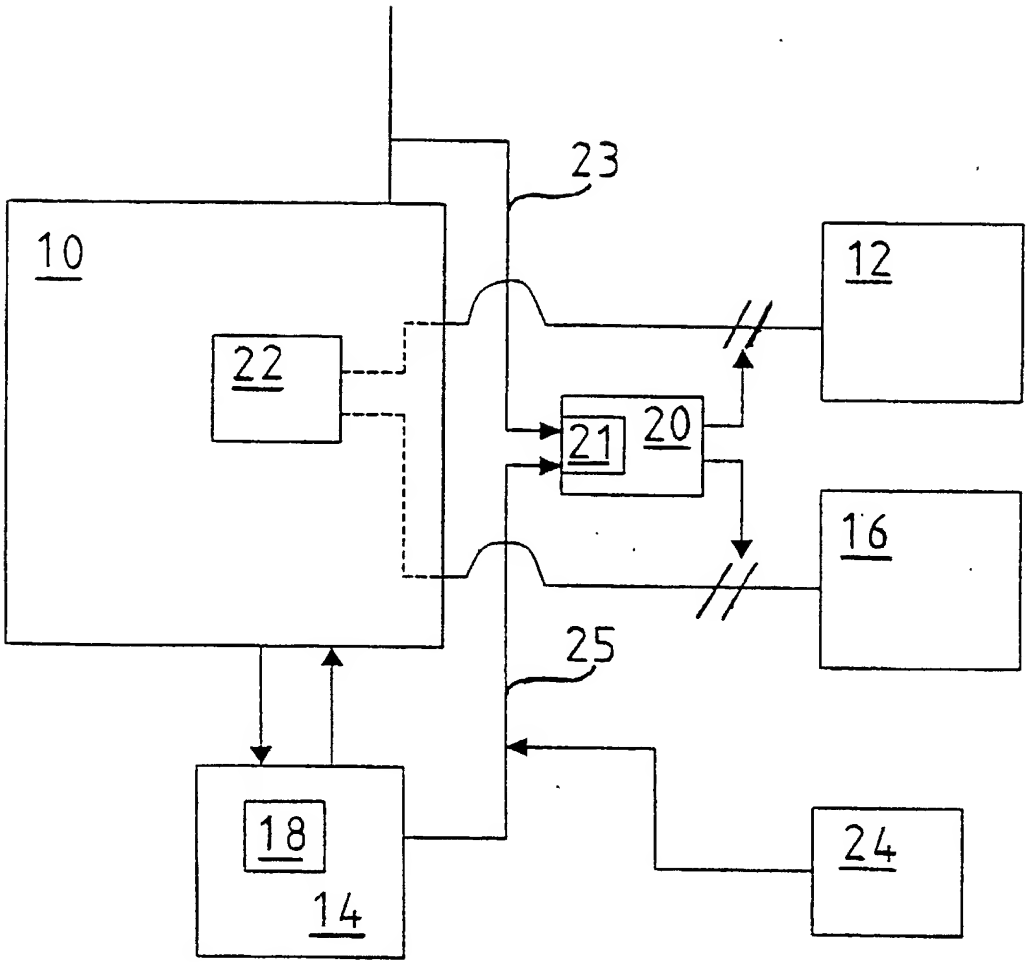

FIG 1

9011 US

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (includes Reference to PCT International Applications)	Attorney's docket No.

55001 US

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A COMPUTER DEVICE WITH A SAFETY FUNCTION

the specification of which (check only one item below):

[ ] is attached hereto.

[ ] was filed as United States application.
Serial No. _____
on _____
and was amended
on _____ (if applicable).

[x] was filed as PCT international application
Number PCT/SE00/01847_____
on 22 September 2000_____
and was amended under PCT Article 19
on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY (if PCT indicate PCT)	APPLICATION NO.	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Sweden	9903422-5	22 September 1999	[x] YES [ ] NO
			[ ] YES [ ] NO
			[ ] YES [ ] NO

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

1008C91 .061002

Combined declaration for patent application and power of attorney (continued) (includes Reference to PCT International Applications)	Attorney's docket No

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:

U.S. APPLICATIONS		STATUS (Check one)		
APPLICATION NO.	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.					
APPLICATION NO.	FILING DATE	US SERIAL NO. ASSIGNED (if any)			
PCT/SE00/01847	22 September 2000				

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number): **Edward A. Pennington (Reg. No. 32,588); John P. Moran (Reg. No. 30,906); Eric J. Franklin (Reg, No. 37,134); Michael A Schwartz (Reg. No. 40,161); Robert C. Bertin (Reg. No. 41,488); Alicia A. Meros (Reg. No. 44,937); Chadwick A. Jackson (Reg. No. 46,495), Edward J. Naidich (Reg. No. 43,826) and Sean O'Hanlon (Reg. No. 47,252)**

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POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
DATE 2002-05-17	DATE 02 05 17	DATE